mechanical polishing (CMP) technique or an etch-back technique. The nitride layer **44** and the pad oxide layer **42** can then be selectively removed using techniques known to those having skill in the art. The resulting structure including the isolation layer **54** in the trench is illustrated in FIG. **4**E. Accordingly, the void formed in the trench can be collapsed and filled, and the etching resistivity of the oxide filling the trench can be increased.

A second method for forming isolation trenches according to the present invention will now be discussed with reference to FIGS. **5**A and **5**B. The pad oxide layer **62** and the nitride layer **64** can be patterned to form a mask exposing an isolation region of the substrate **60** as discussed above with regard to FIG. **4**A. The trench can be formed by anisotropic etching and an undoped oxide layer **66** can be deposited thereon by chemical vapor deposition (CVD) techniques. As shown, this undoped oxide layer **66** can cover the surface of the substrate and fill the trench. A void **68**, however, may be formed in the oxide in the trench. The thickness of this undoped oxide layer **66** should be sufficient to fill the trench when the oxide layer is reflowed.

The undoped oxide layer **66** can be implanted with impurity ions as shown in FIG. **5**B. In particular, the undoped oxide layer **66** can be implanted with impurity ions such as boron (B^+) ions, phosphorous (P^+) ions, or difluoroborate (BF_2^+) ions which can allow the oxide layer **66** to reflow when heated. The concentration of boron or phosphorous in a boro-silicate glass (BSG), a phospho-silicate glass (PSG), or a borophosphorous-silicate glass (BPSG) as discussed above with regard to FIG. **4**B may be on the order of 1×10^{20} ions/cm^2. Accordingly, to achieve a sufficient concentration of boron and/or phosphorous in the undoped oxide layer of FIG. **5**A, the implant dose should be about $1\times10_{15}$ to 1×10^{17} ions/cm^2. In addition, the implant energy should be controlled to provide an average implant range Rp**2** for the implanted ions into the mask layer. As shown in FIG. **5**B, the implant range is preferably sufficiently deep so that silicon will be able to reflow to fill the void **68**, and the implant range may extend into the nitride layer **64** over the active regions of the substrate and into portions of the oxide adjacent the void. The implant energy, however, should not be made so high that the substrate is doped.

The isolation trench structure can be completed as discussed above with regard to FIGS. **4**C–**4**E. That is, the implanted portion of the oxide layer **66** can be reflowed by a thermal process to fill the void **68**. The reflowed oxide layer can then be implanted to increase an etch resistivity thereof. The oxide layer can then be planarized, and the nitride layer **64** and the oxide layer **62** can be selectively removed.

According to the trench isolation methods of the present invention, an oxide can be deposited in a trench and implanted to decrease an etch rate of the oxide layer. This decreased etch rate allows the selective removal of mask layers without removing excessive portions of the oxide filling the trench. In addition, an undoped oxide layer can be deposited and implanted to allow the oxide to reflow to fill a void formed therein. Accordingly, the step of forming a barrier layer to prevent the diffusion of impurity ions in the substrate can be omitted. In other words, by implanting only a surface portion of the oxide layer, a single oxide deposition can be used to form the isolation trench structure.

In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

That which is claimed is:

1. A method for forming a microelectronic structure, said method comprising the steps of:

forming a trench in a substrate;

forming an insulating layer in said trench and covering said substrate;

in implanting ions into said insulating layer which decrease an etch rate of said insulating layer; and

removing portions of said insulating layer on said substrate while maintaining said insulating layer in said trench;

wherein said step of forming said insulating layer comprises forming an undoped oxide layer on said substrate, and forming a doped oxide layer on said undoped oxide layer wherein a void is formed in said doped oxide layer in said trench.

2. A method according to claim **1** wherein said implanting step comprises implanting nitrogen (N^+) ions.

3. A method according to claim **2** wherein said nitrogen ions are implanted at a dose on the order of 1×10^{13} to 1×10^{18} ions/cm^2.

4. A method according to claim **1** wherein said step of forming said doped oxide layer is followed by reflowing said doped oxide layer wherein said reflowing step reduces said void.

5. A method according to claim **4** wherein said reflowing step comprises heating said insulating layer to a temperature of about 950° C. to 1,150° C.

6. A method according to claim **1** wherein said doped oxide layer comprises a material chosen from the group consisting of boro-silicate glass (BSG), phospho-silicate glass (PSG), and borophosphorous-silicate glass (BPSG).

7. A method according to claim **1** wherein said step of forming said trench is preceded by the step of forming a mask layer on said substrate wherein said mask layer exposes a portion of said substrate, wherein said trench is formed in said exposed portion of said substrate, wherein said insulating layer covers said mask layer, and wherein said removing step comprises removing portions of said insulating layer on said mask layer and removing said mask layer.

8. A method for forming a microelectronic structure, said method comprising the steps of:

forming a trench in a substrate;

forming an insulating layer which fills said trench and covers said substrate wherein a void is formed in said insulating layer in said trench;

implanting ions into said insulating layer; and

reflowing said implanted insulating layer wherein said reflowing step reduces said void.

9. A method according to claim **8** wherein said implanting step comprises implanting ions chosen from the group consisting of boron (B^+) ions, phosphorous (P^+) ions, and difluoroborate (BF_2^+) ions.

10. A method according to claim **9** wherein said implanted ions are implanted at a dose on the order of 1×10^{15} to 1×10^{17} ions/cm^2.

11. A method according to claim **8** wherein said reflowing step comprises heating said insulating layer to a temperature of about 950° C. to 1,500° C.

12. A method according to claim **8** wherein said insulating layer comprises an undoped oxide layer.

13. A method according to claim **8** further comprising the step of implanting nitrogen (N^+) ions into said insulating layer which decrease an etch rate of said insulating layer.